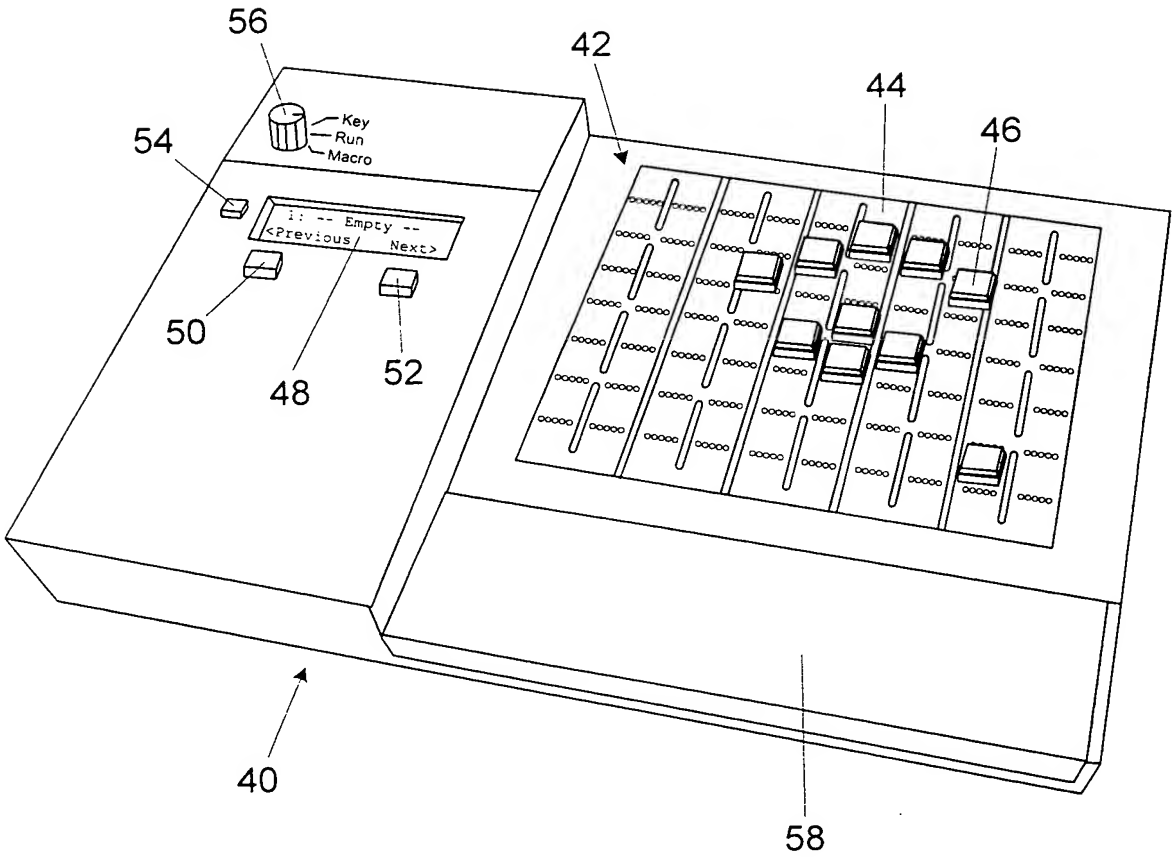

Fig. 1

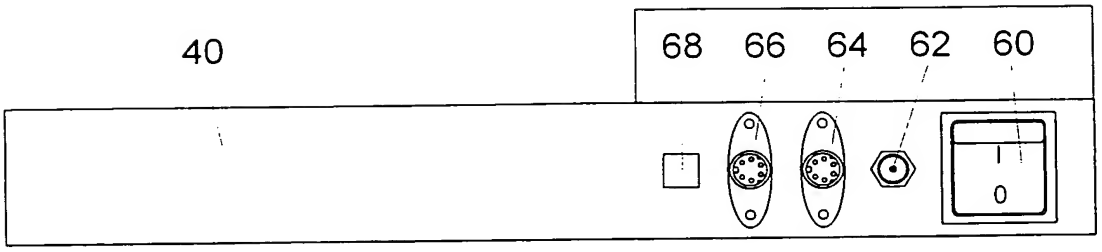

Fig. 2

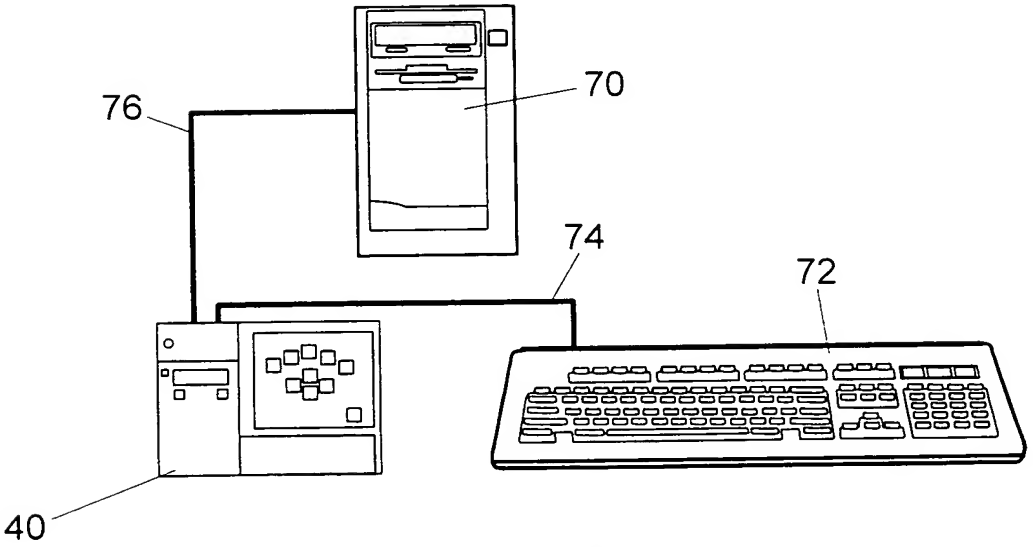

Fig. 3

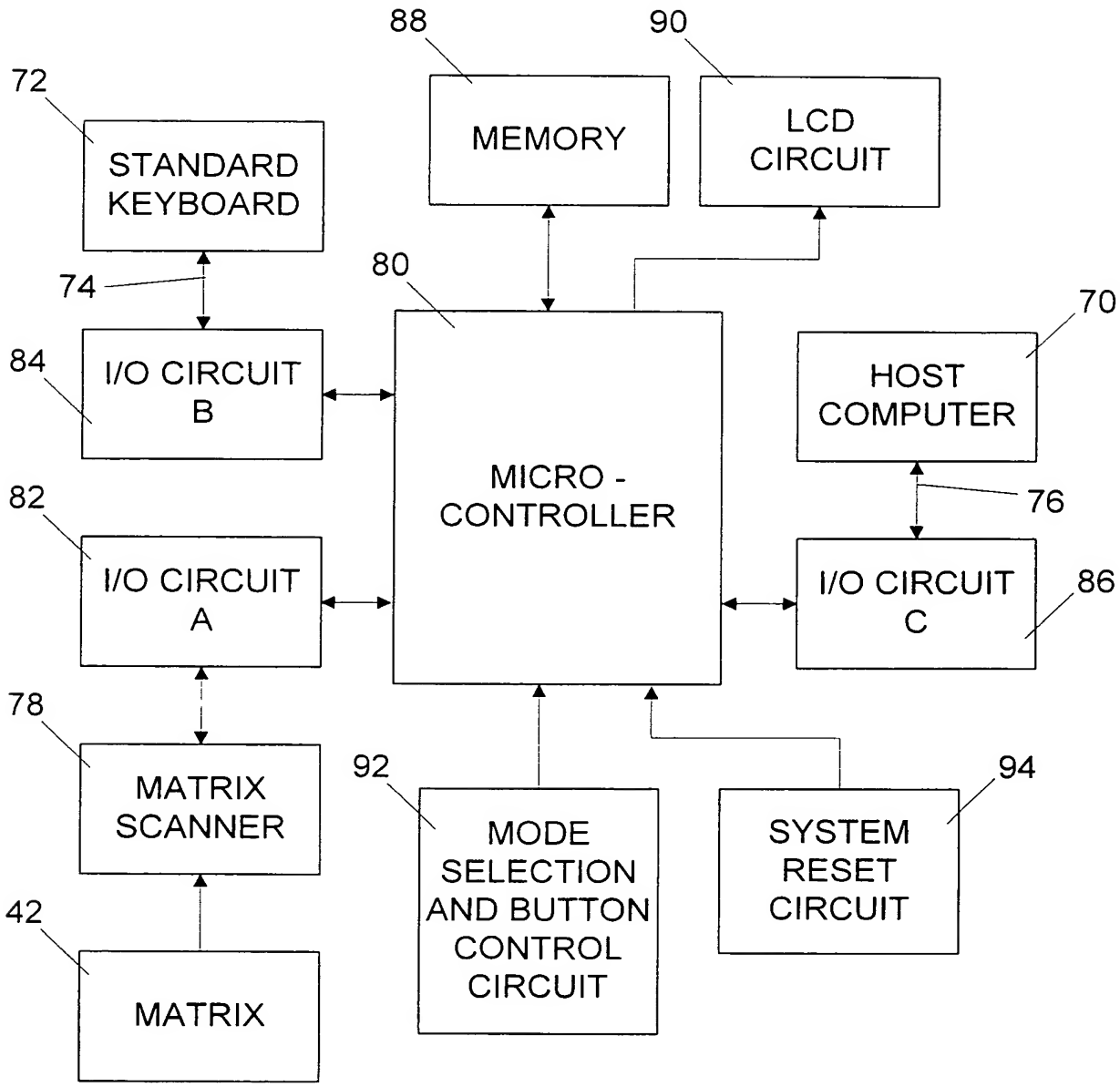
88
90
72
MEMORY
LCD CIRCUIT
STANDARD KEYBOARD
74
80
70
84
I/O CIRCUIT B
HOST COMPUTER
MICRO - CONTROLLER
82
76
I/O CIRCUIT A
I/O CIRCUIT C
86
78
92
94
MATRIX SCANNER
MODE SELECTION AND BUTTON CONTROL CIRCUIT
SYSTEM RESET CIRCUIT
42
MATRIX

Fig. 4

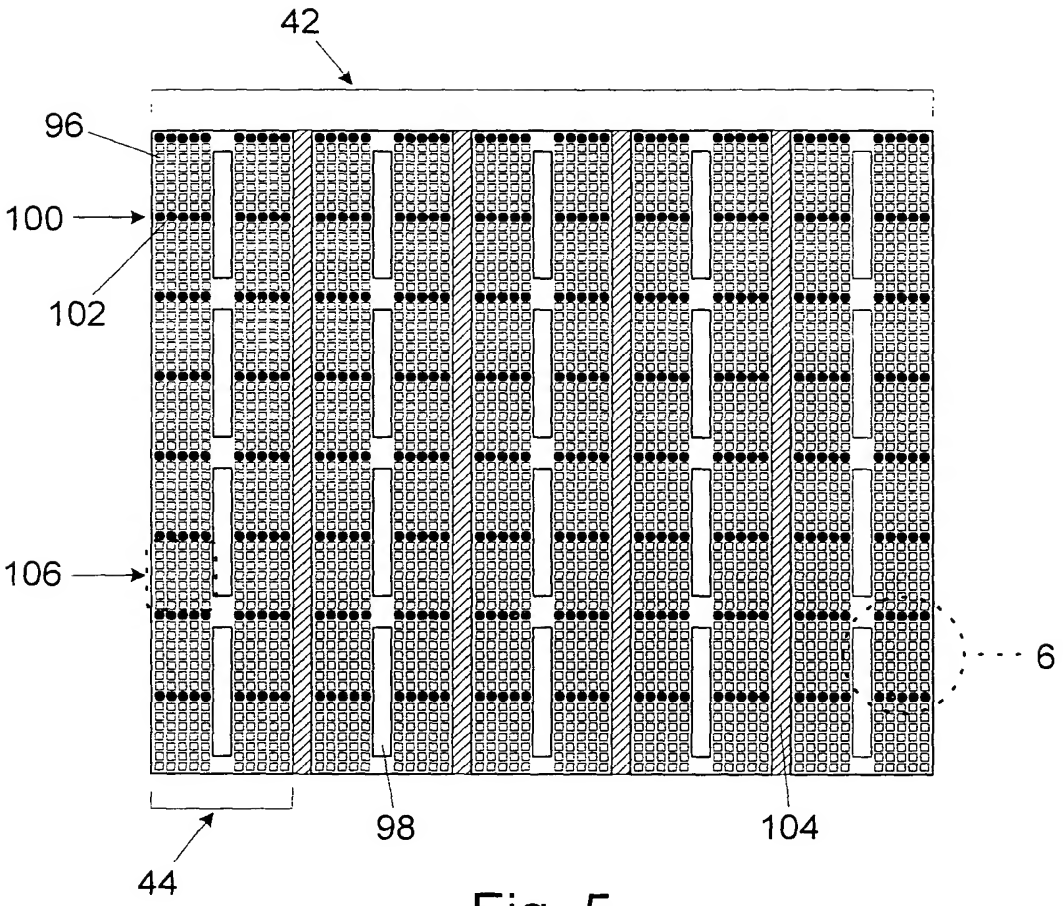
42
96
100
102
106
6
98
104
44

Fig. 5

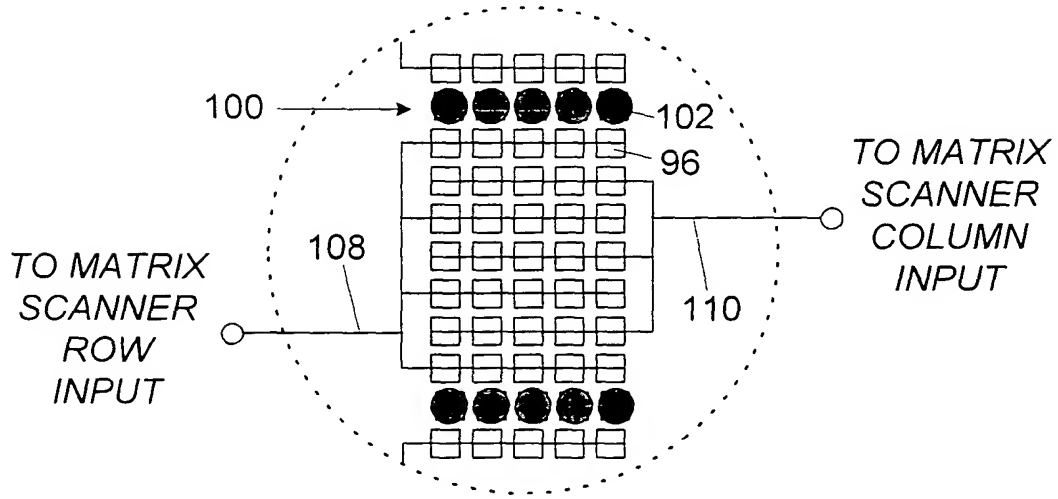
100
102
96
TO MATRIX SCANNER COLUMN INPUT
108
110
TO MATRIX SCANNER ROW INPUT

Fig. 6

Fig. 7

112
114
116
118

9 46 R: 2 C: 4	- 4E R: 1 C: 3	; 4C R: 0 C: 3	CAPS 58 R: 4 C: 10	F3 04 R: 4 C: 8	I 43 R: 3 C: 5	U 3C R: 3 C: 6	M 3A R: 6 C: 6	PAD * 7C R: 6 C: 15	R 2D R: 3 C: 7
ESC 76 R: 5 C: 11	F 2B R: 0 C: 7	F1 05 R: 1 C: 10	F10 09 R: 2 C: 2	PAD 2 72 R: 0 C: 12	PAD 3 7A R: 0 C: 15	PAD 4 6B R: 4 C: 9	PAD 5 73 R: 4 C: 12	X 22 R: 6 C: 10	Y 35 R: 4 C: 6
Z 1A R: 6 C: 11	D 23 R: 0 C: 8	E 24 R: 3 C: 8	RET 5A R: 6 C: 2	PAD . 71 R: 5 C: 15	PAD + 79 R: 3 C: 16	PAD 0 70 R: 5 C: 12	PAD 1 69 R: 0 C: 9	V 2A R: 6 C: 7	W 1D R: 3 C: 10
= 55 R: 1 C: 5	A 1C R: 0 C: 11	B 32 R: 7 C: 7	BACK 66 R: 4 C: 2	N 31 R: 7 C: 6	O 44 R: 3 C: 4	P 4D R: 3 C: 3	PAD - 7B R: 7 C: 15	T 2C R: 4 C: 7	Tab 0D R: 4 C: 11
/ 4A R: 7 C: 3	[54 R: 4 C: 3	] 5B R: 4 C: 5	~ 0E R: 1 C: 11	K 42 R: 0 C: 5	L 4B R: 0 C: 4	L ALT 11 R: 5 C: 1	L CTR 14 R: 1 C: 17	SCR 7E R: 3 C: 1	SPA 29 R: 7 C: 2
8 3E R: 2 C: 5	' 52 R: 5 C: 3	\ 5D R: 0 C: 2	. 49 R: 6 C: 4	NUM 77 R: 6 C: 9	G 34 R: 5 C: 7	H 33 R: 5 C: 6	J 3B R: 0 C: 6	Q 15 R: 3 C: 11	S 1B R: 0 C: 10
4 25 R: 2 C: 7	5 2E R: 1 C: 7	6 36 R: 1 C: 6	7 3D R: 2 C: 6	F5 03 R: 5 C: 2	F6 0B R: 5 C: 5	F7 83 R: 4 C: 4	F8 0A R: 1 C: 4	PAD 8 75 R: 3 C: 12	PAD 9 7D R: 3 C: 15
0 45 R: 2 C: 3	1 16 R: 2 C: 11	2 1E R: 2 C: 10	3 26 R: 2 C: 8	F11 78 R: 2 C: 9	F12 07 R: 2 C: 12	F2 06 R: 1 C: 8	F4 0C R: 5 C: 8	PAD 6 74 R: 4 C: 15	PAD 7 6C R: 3 C: 9

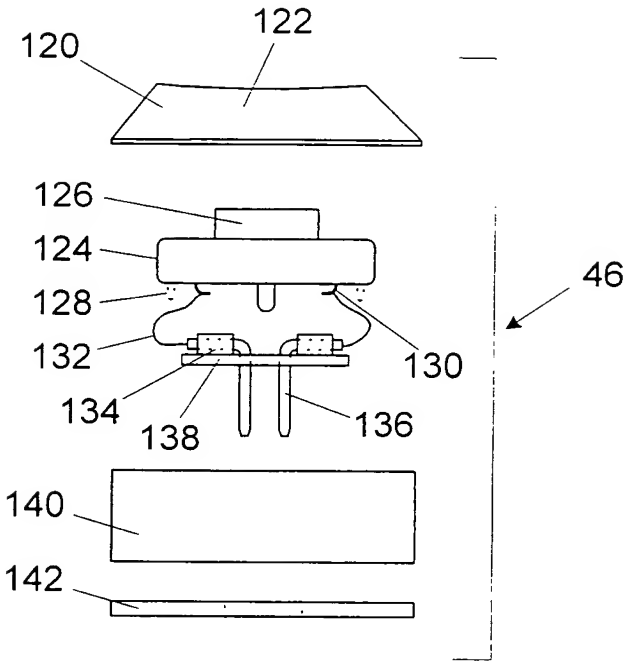
120
122
126
124
128
132
130
134
138
136
140
142
46

Fig. 8A

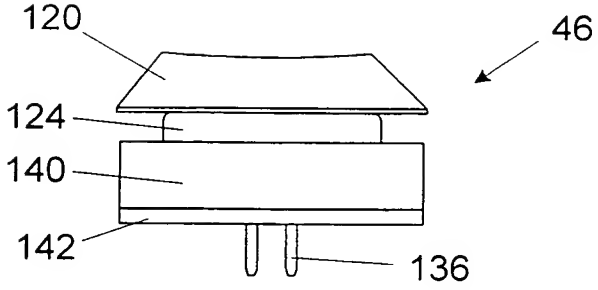
120
46
124
140
142
136

Fig. 8B

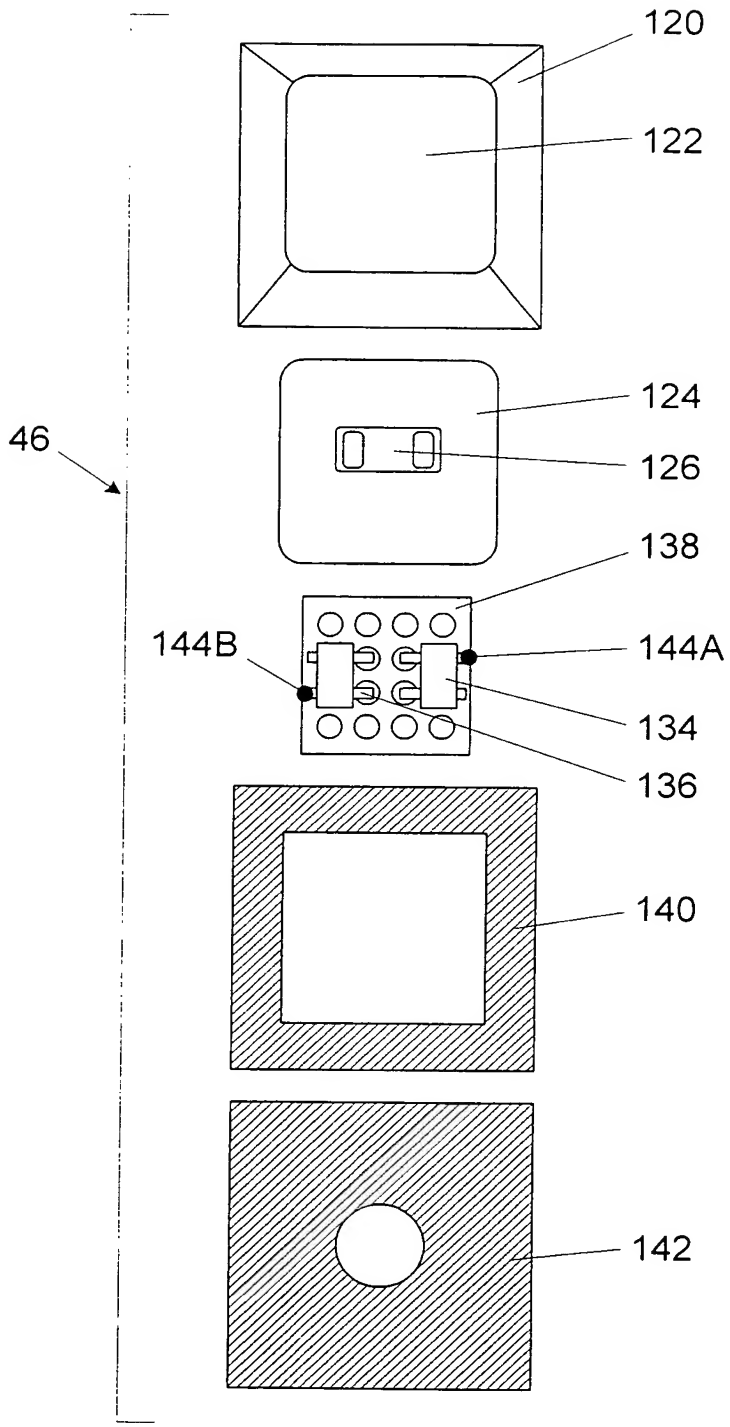

Fig. 8C

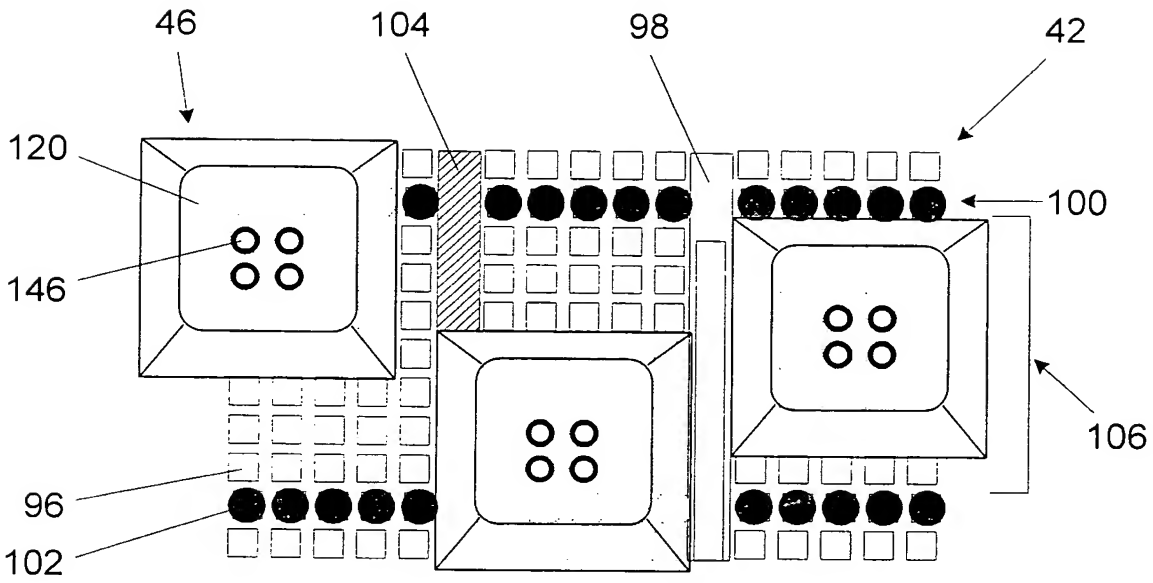

Fig. 9

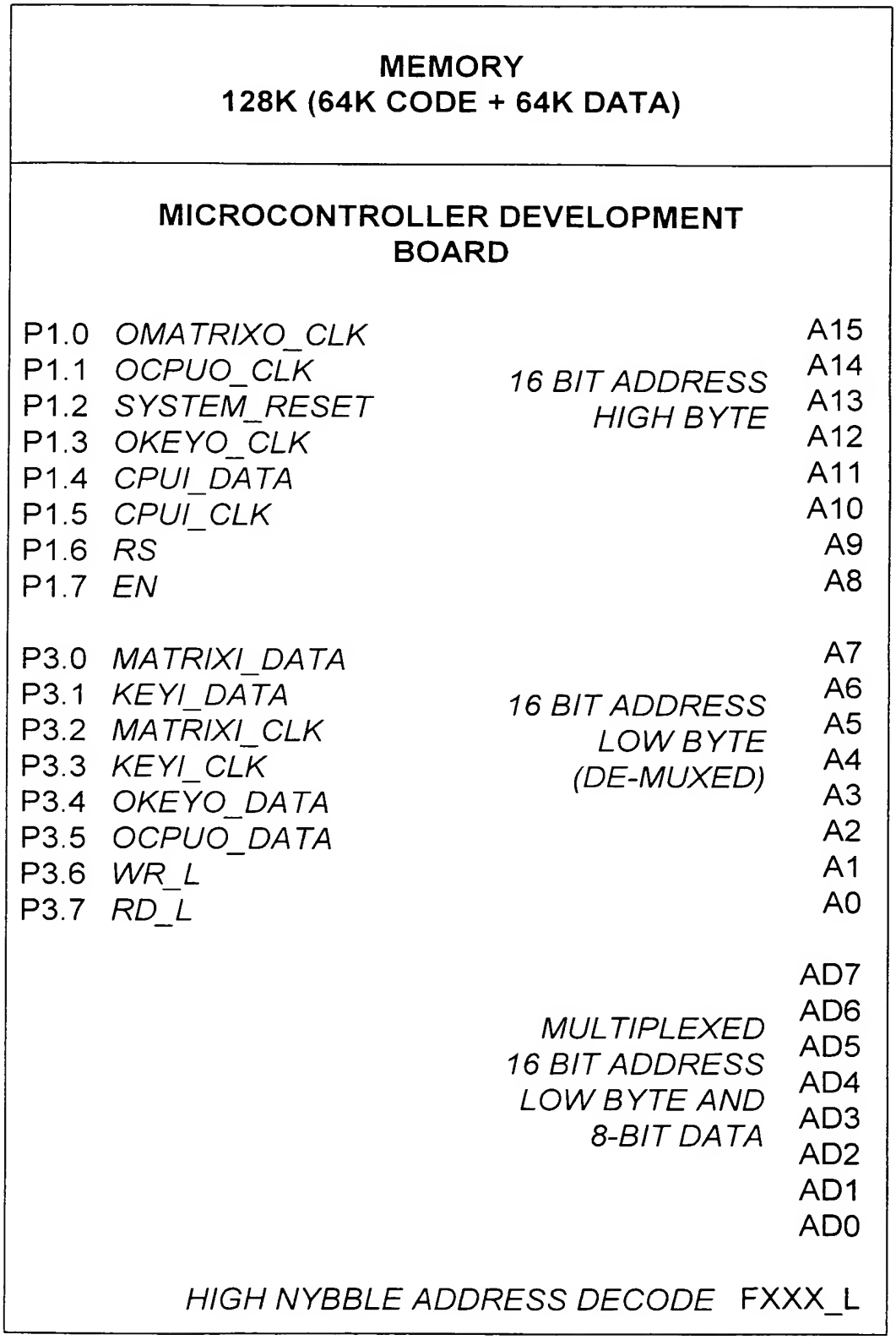
MEMORY
128K (64K CODE + 64K DATA)
MICROCONTROLLER DEVELOPMENT BOARD
P1.0 OMATRIXO_CLK
P1.1 OCPUO_CLK
P1.2 SYSTEM_RESET
P1.3 OKEYO_CLK
P1.4 CPUI_DATA
P1.5 CPUI_CLK
P1.6 RS
P1.7 EN
16 BIT ADDRESS HIGH BYTE
A15
A14
A13
A12
A11
A10
A9
A8
P3.0 MATRIXI_DATA
P3.1 KEYI_DATA
P3.2 MATRIXI_CLK
P3.3 KEYI_CLK
P3.4 OKEYO_DATA
P3.5 OCPUO_DATA
P3.6 WR_L
P3.7 RD_L
16 BIT ADDRESS LOW BYTE (DE-MUXED)
A7
A6
A5
A4
A3
A2
A1
A0
MULTIPLEXED 16 BIT ADDRESS LOW BYTE AND 8-BIT DATA
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
HIGH NYBBLE ADDRESS DECODE FXXX_L

Fig. 10

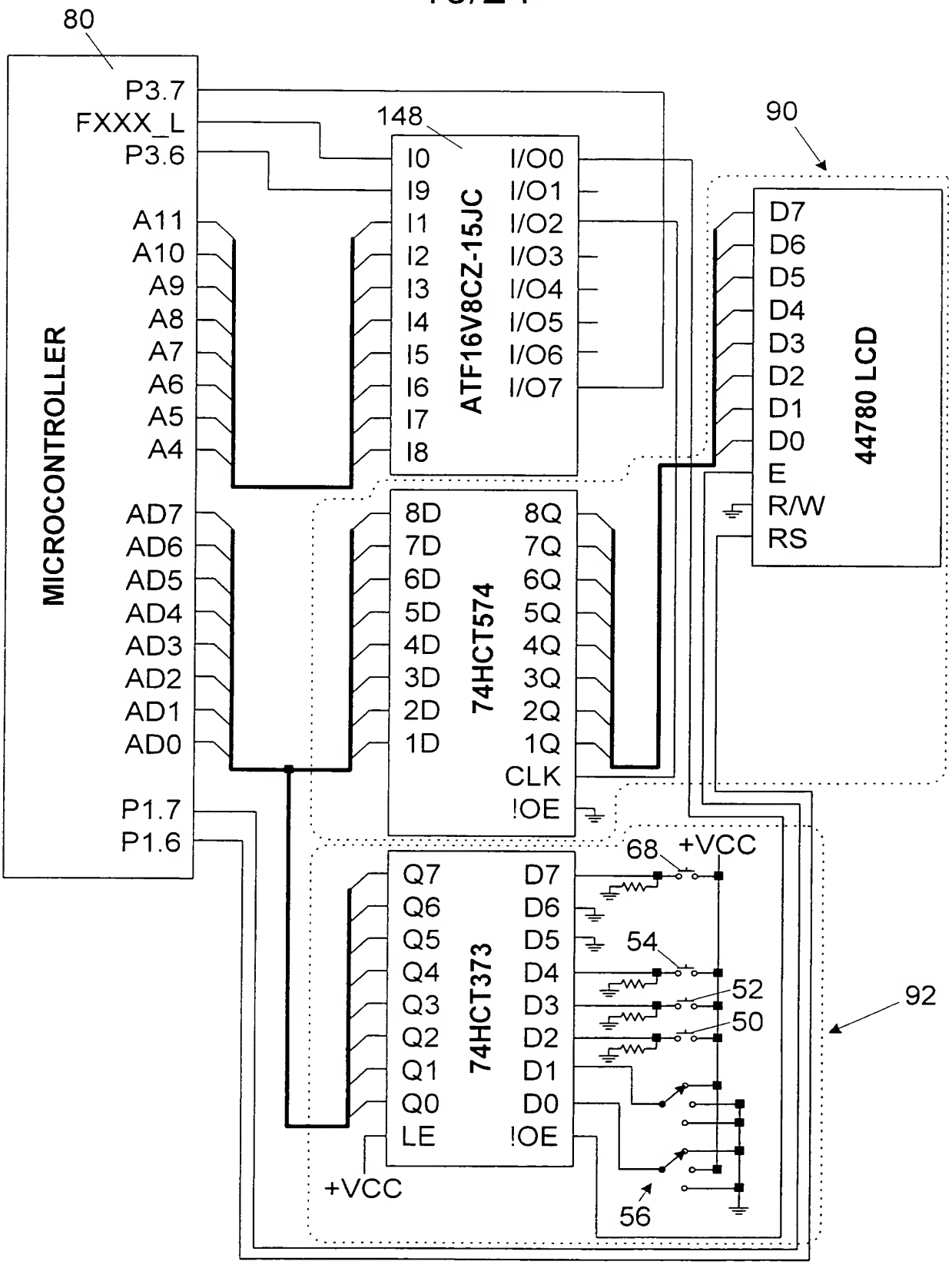
80
MICROCONTROLLER
P3.7
FXXX_L
P3.6
A11
A10
A9
A8
A7
A6
A5
A4
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
P1.7
P1.6
148
ATF16V8CZ-15JC
I0
I9
I1
I2
I3
I4
I5
I6
I7
I8
I/O0
I/O1
I/O2
I/O3
I/O4
I/O5
I/O6
I/O7
90
44780 LCD
D7
D6
D5
D4
D3
D2
D1
D0
E
R/W
RS
74HCT574
8D
7D
6D
5D
4D
3D
2D
1D
8Q
7Q
6Q
5Q
4Q
3Q
2Q
1Q
CLK
!OE
74HCT373
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
LE
D7
D6
D5
D4
D3
D2
D1
D0
!OE
+VCC
68
+VCC
54
52
50
92
56

Fig. 11

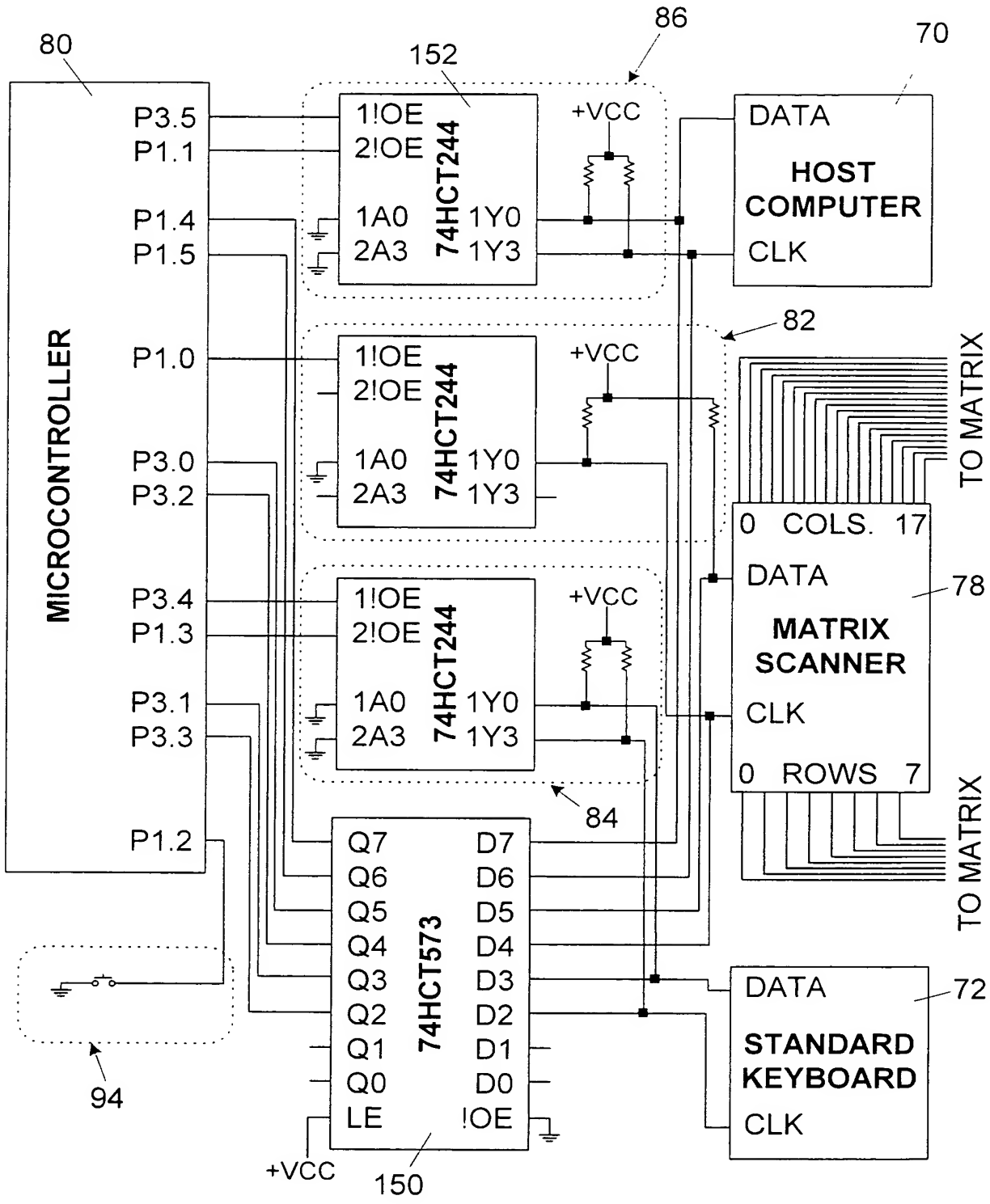
80
MICROCONTROLLER
P3.5
P1.1
P1.4
P1.5
P1.0
P3.0
P3.2
P3.4
P1.3
P3.1
P3.3
P1.2
86
152
1!OE
2!OE
1A0
2A3
74HCT244
1Y0
1Y3
+VCC
82
84
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
LE
D7
D6
D5
D4
D3
D2
D1
D0
!OE
74HCT573
+VCC
150
94
70
DATA
HOST COMPUTER
CLK
TO MATRIX
0 COLS. 17
DATA
MATRIX SCANNER
CLK
0 ROWS 7
78
TO MATRIX
DATA
STANDARD KEYBOARD
CLK
72

Fig. 12

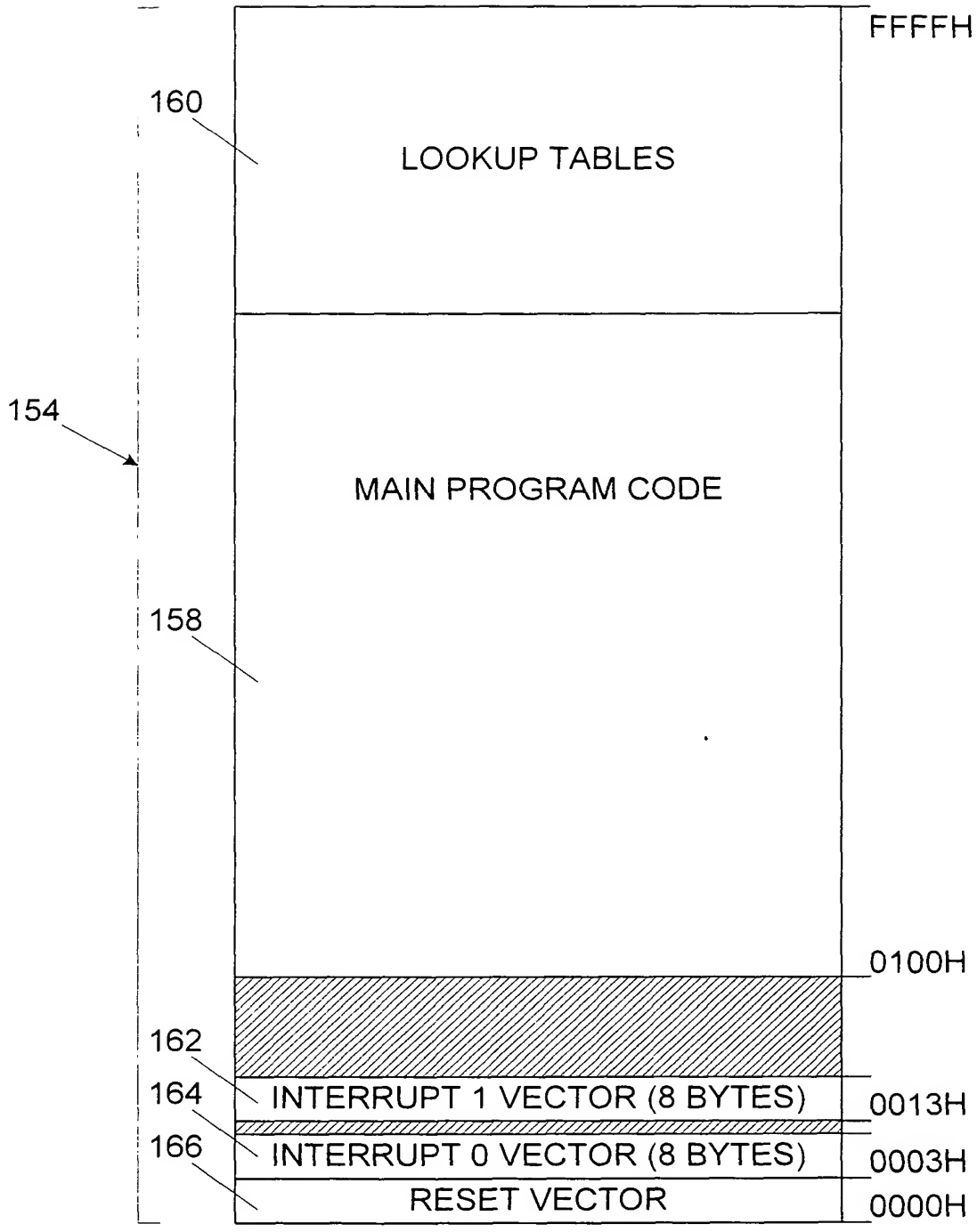
FFFFH
160
LOOKUP TABLES
154
MAIN PROGRAM CODE
158
0100H
162
INTERRUPT 1 VECTOR (8 BYTES)
0013H
164
INTERRUPT 0 VECTOR (8 BYTES)
0003H
166
RESET VECTOR
0000H

Fig. 13

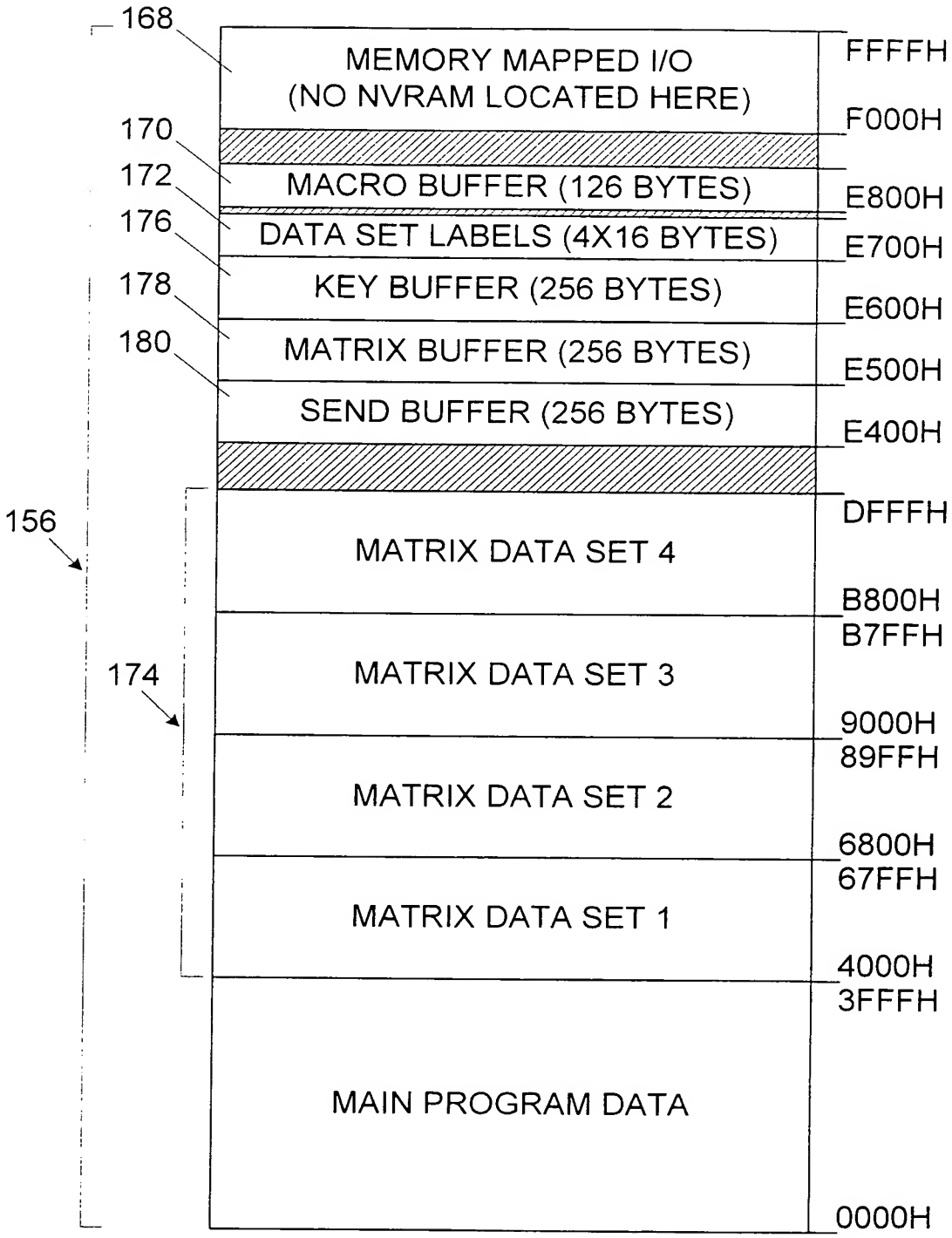
168
MEMORY MAPPED I/O
(NO NVRAM LOCATED HERE)
FFFFH
F000H
170
172
MACRO BUFFER (126 BYTES)
E800H
176
DATA SET LABELS (4X16 BYTES)
E700H
178
KEY BUFFER (256 BYTES)
E600H
180
MATRIX BUFFER (256 BYTES)
E500H
SEND BUFFER (256 BYTES)
E400H
156
DFFFH
MATRIX DATA SET 4
B800H
B7FFH
174
MATRIX DATA SET 3
9000H
89FFH
MATRIX DATA SET 2
6800H
67FFH
MATRIX DATA SET 1
4000H
3FFFH
MAIN PROGRAM DATA
0000H

Fig. 14

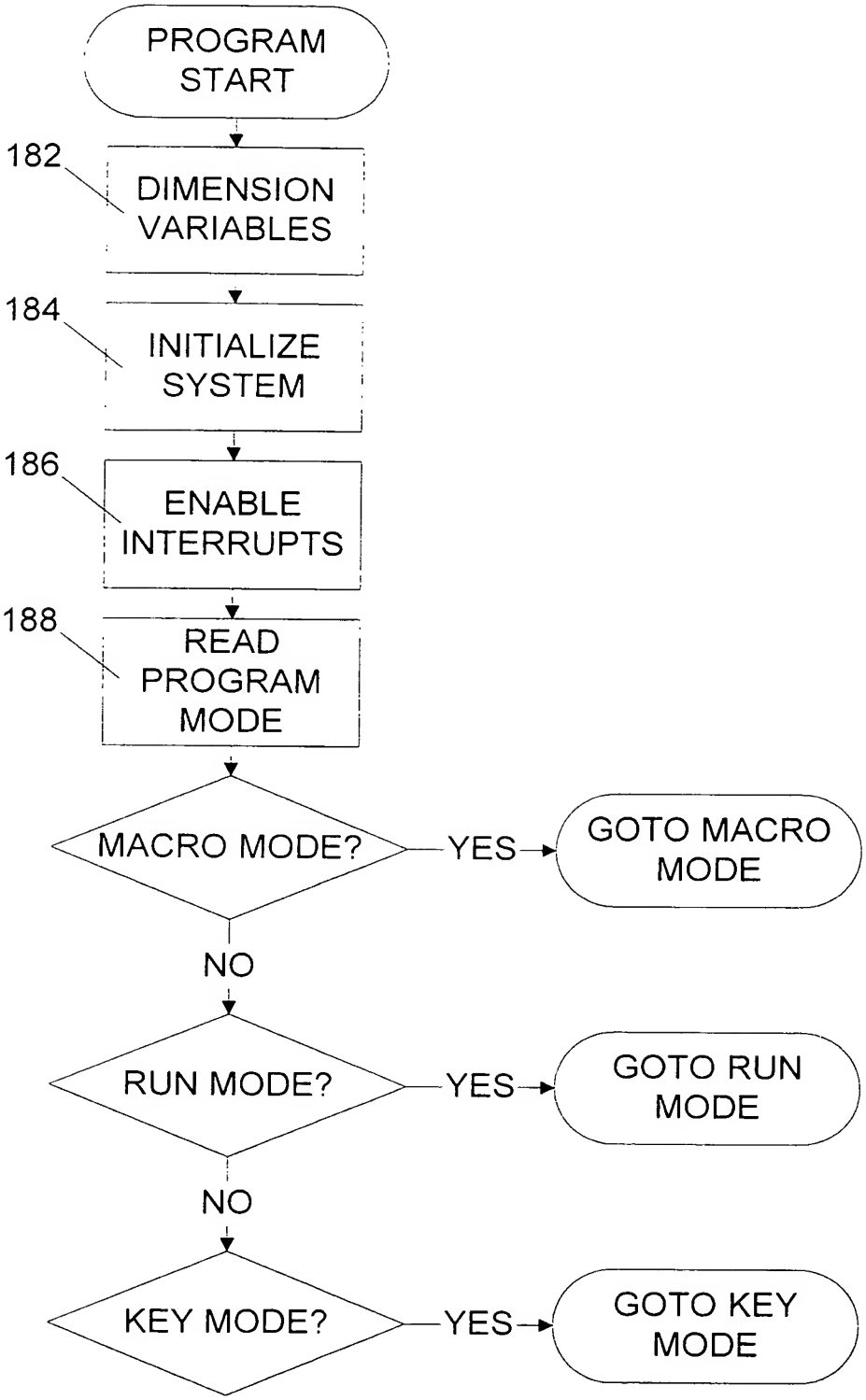
PROGRAM START
182
DIMENSION VARIABLES
184
INITIALIZE SYSTEM
186
ENABLE INTERRUPTS
188
READ PROGRAM MODE
MACRO MODE?
YES
GOTO MACRO MODE
NO
RUN MODE?
YES
GOTO RUN MODE
NO
KEY MODE?
YES
GOTO KEY MODE

Fig. 15

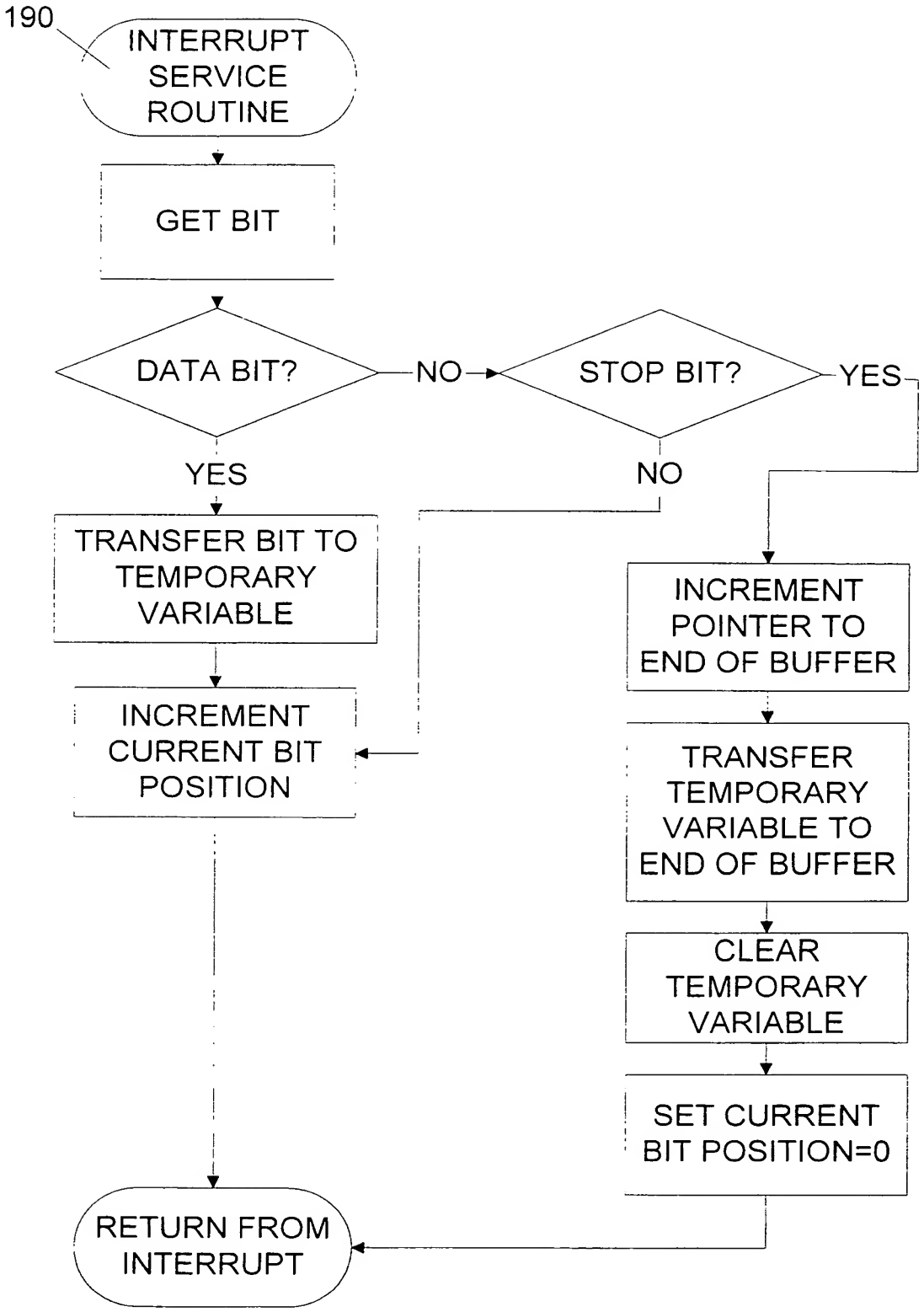
190
INTERRUPT SERVICE ROUTINE
GET BIT
DATA BIT?
NO
STOP BIT?
YES
YES
NO
TRANSFER BIT TO TEMPORARY VARIABLE
INCREMENT CURRENT BIT POSITION
INCREMENT POINTER TO END OF BUFFER
TRANSFER TEMPORARY VARIABLE TO END OF BUFFER
CLEAR TEMPORARY VARIABLE
SET CURRENT BIT POSITION=0
RETURN FROM INTERRUPT

Fig. 16

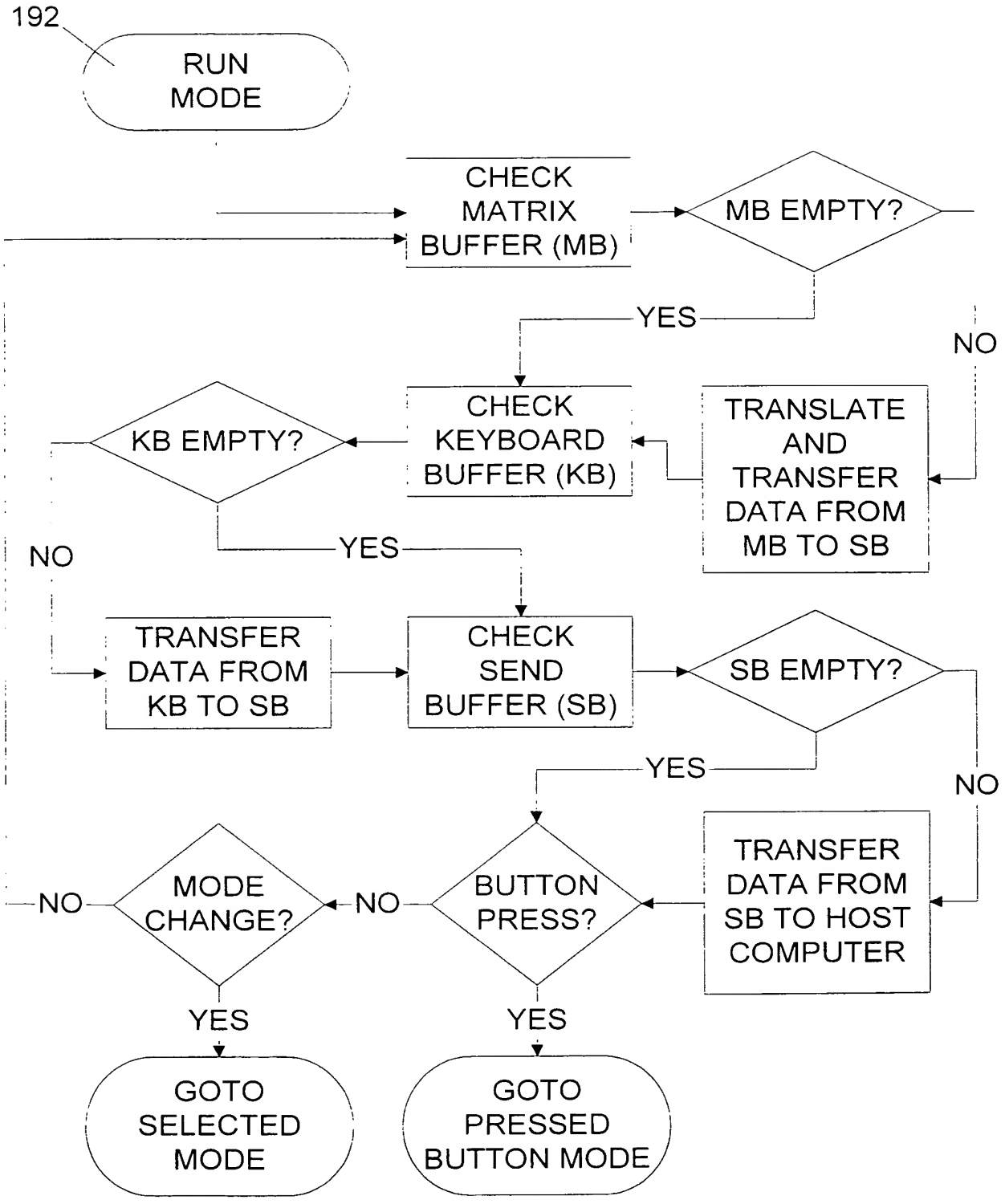
192
RUN MODE
CHECK MATRIX BUFFER (MB)
MB EMPTY?
YES
NO
CHECK KEYBOARD BUFFER (KB)
KB EMPTY?
TRANSLATE AND TRANSFER DATA FROM MB TO SB
NO
YES
TRANSFER DATA FROM KB TO SB
CHECK SEND BUFFER (SB)
SB EMPTY?
YES
NO
TRANSFER DATA FROM SB TO HOST COMPUTER
BUTTON PRESS?
MODE CHANGE?
NO
NO
YES
YES
GOTO SELECTED MODE
GOTO PRESSED BUTTON MODE

Fig. 17

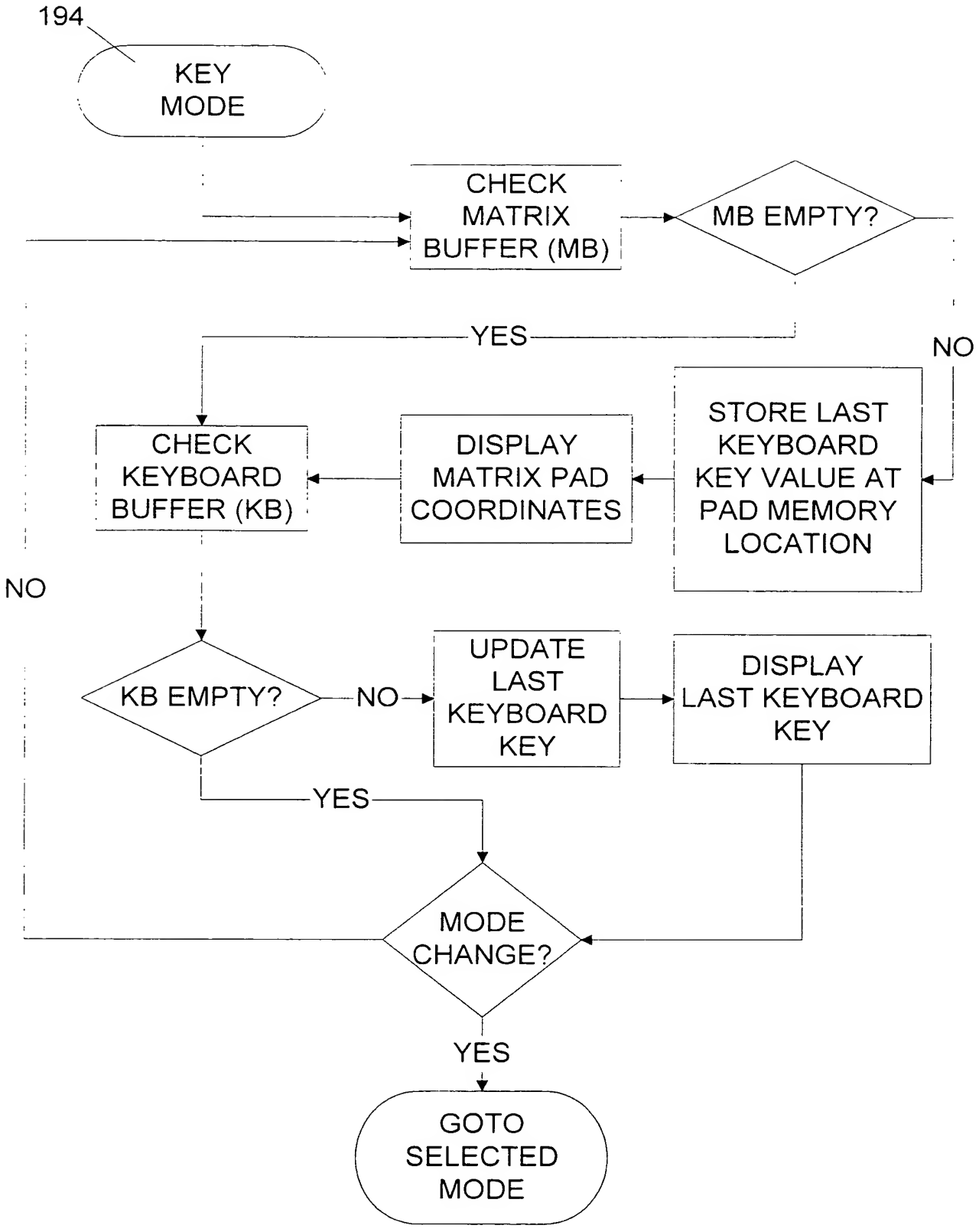
194
KEY MODE
CHECK MATRIX BUFFER (MB)
MB EMPTY?
YES
NO
CHECK KEYBOARD BUFFER (KB)
DISPLAY MATRIX PAD COORDINATES
STORE LAST KEYBOARD KEY VALUE AT PAD MEMORY LOCATION
NO
KB EMPTY?
NO
UPDATE LAST KEYBOARD KEY
DISPLAY LAST KEYBOARD KEY
YES
MODE CHANGE?
YES
GOTO SELECTED MODE

Fig. 18

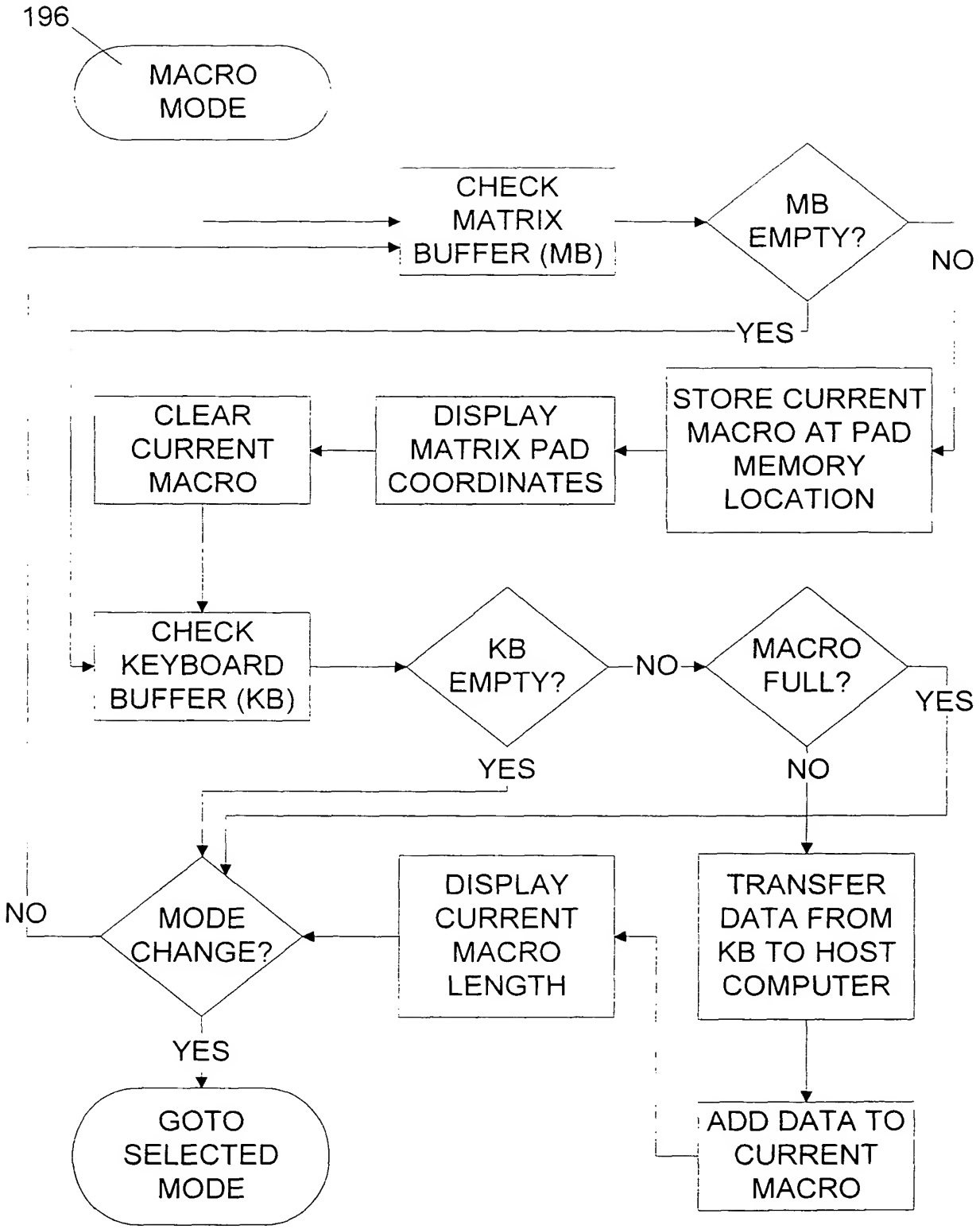
196
MACRO MODE
CHECK MATRIX BUFFER (MB)
MB EMPTY?
NO
YES
STORE CURRENT MACRO AT PAD MEMORY LOCATION
DISPLAY MATRIX PAD COORDINATES
CLEAR CURRENT MACRO
CHECK KEYBOARD BUFFER (KB)
KB EMPTY?
NO
MACRO FULL?
YES
YES
NO
NO
MODE CHANGE?
DISPLAY CURRENT MACRO LENGTH
TRANSFER DATA FROM KB TO HOST COMPUTER
YES
GOTO SELECTED MODE
ADD DATA TO CURRENT MACRO

Fig. 19

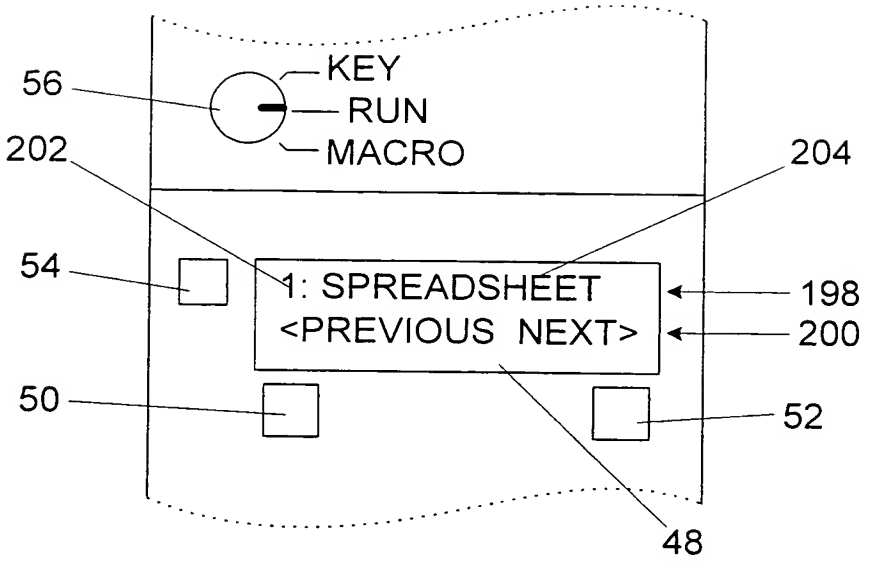

Fig. 20A

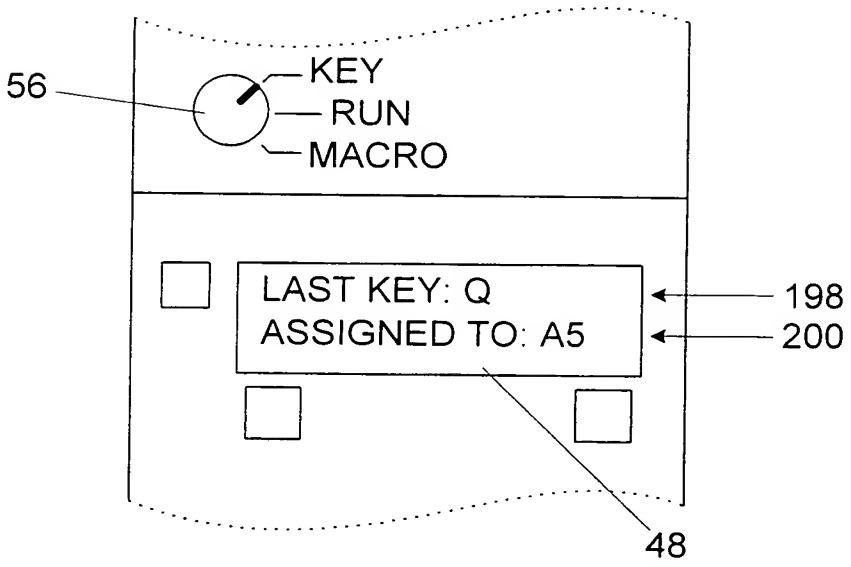

Fig. 20B

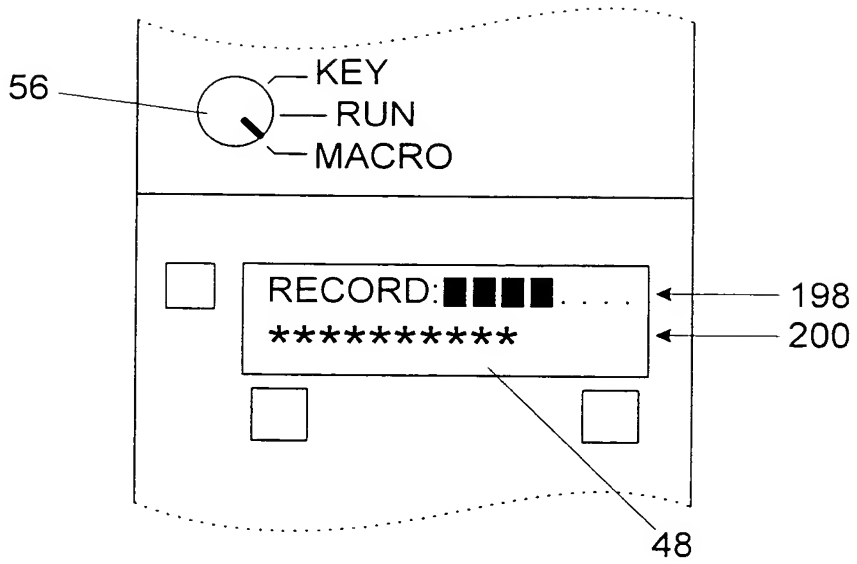

Fig. 20C

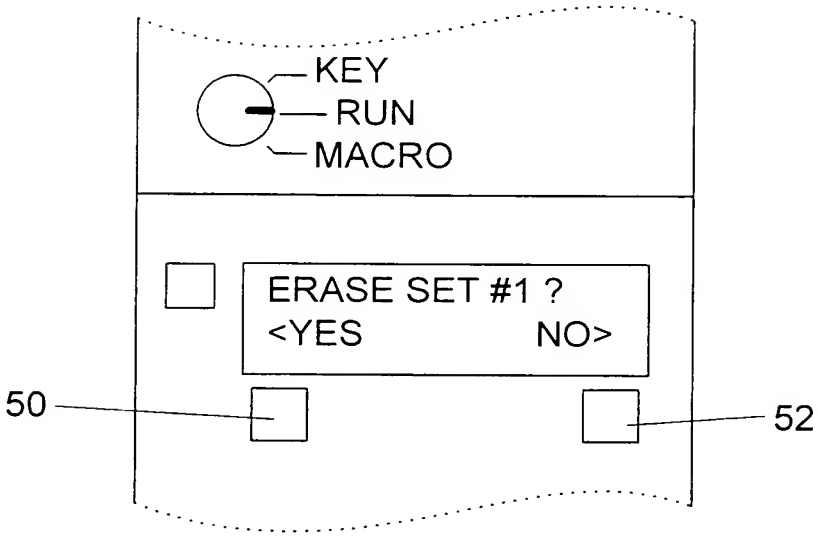

Fig. 20D

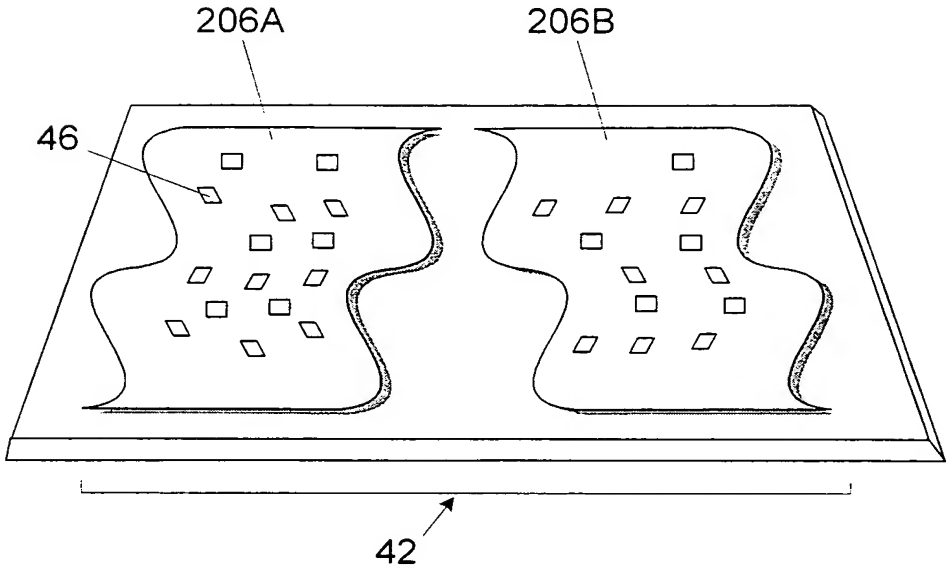

Fig. 21

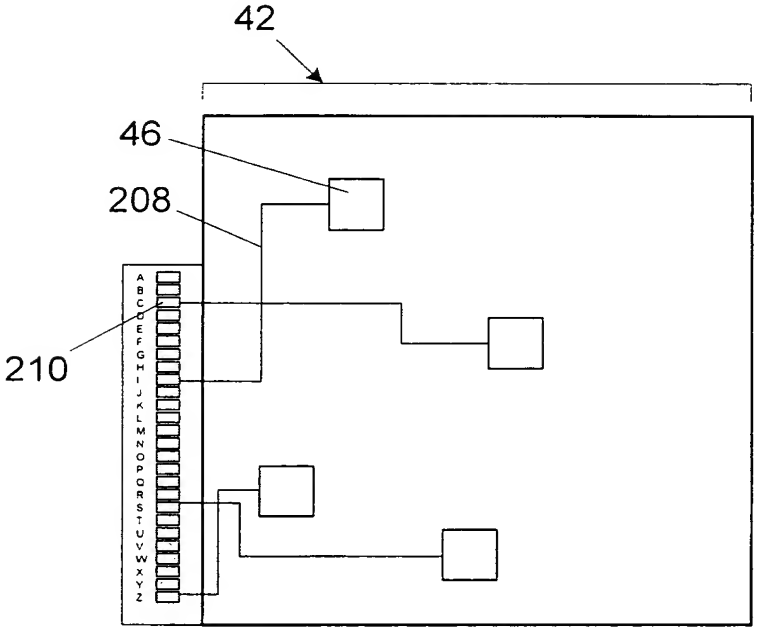

Fig. 22

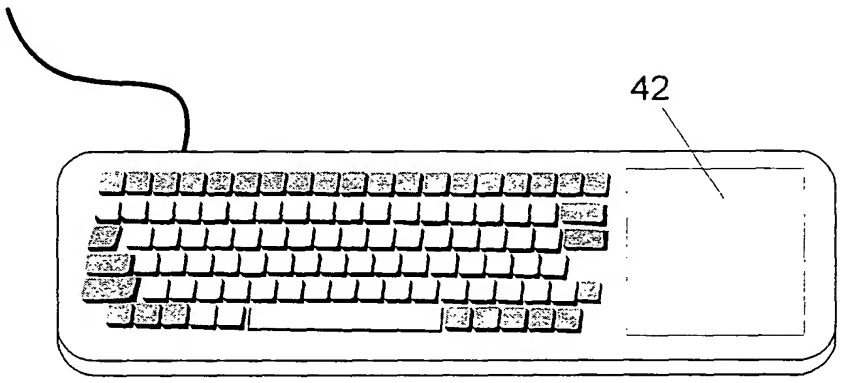

Fig. 23

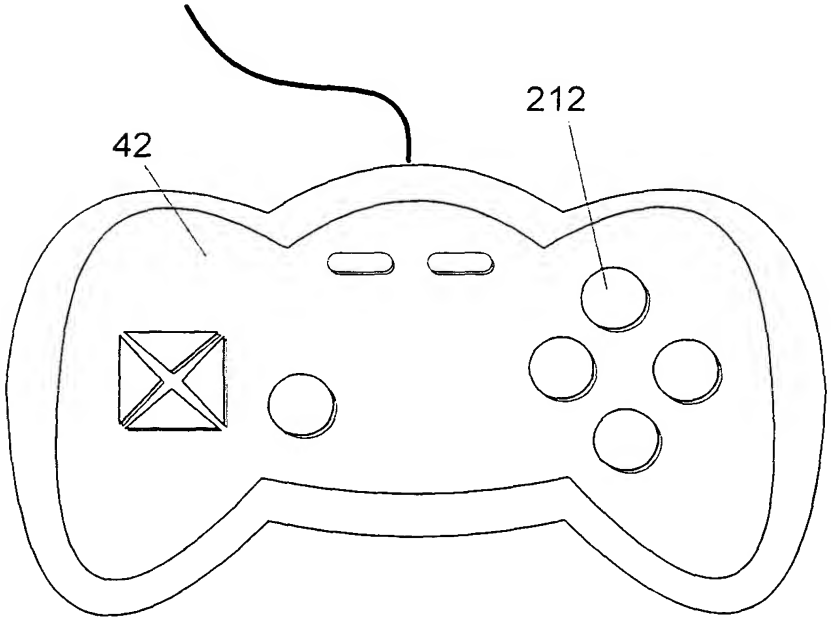

Fig. 24

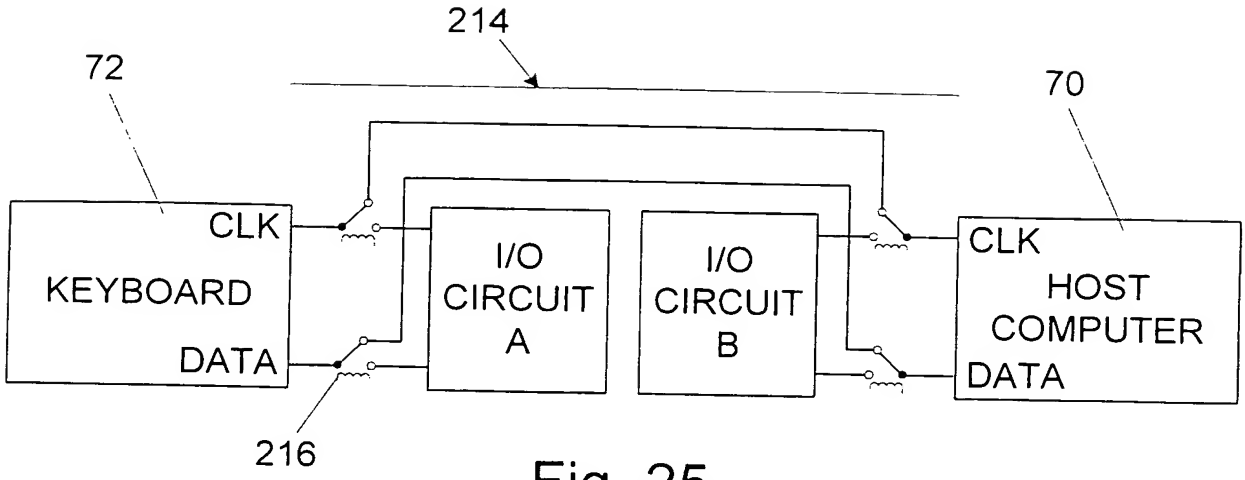
214
72
70
CLK
KEYBOARD
DATA
I/O
CIRCUIT
A
I/O
CIRCUIT
B
CLK
HOST
COMPUTER
DATA
216

Fig. 25

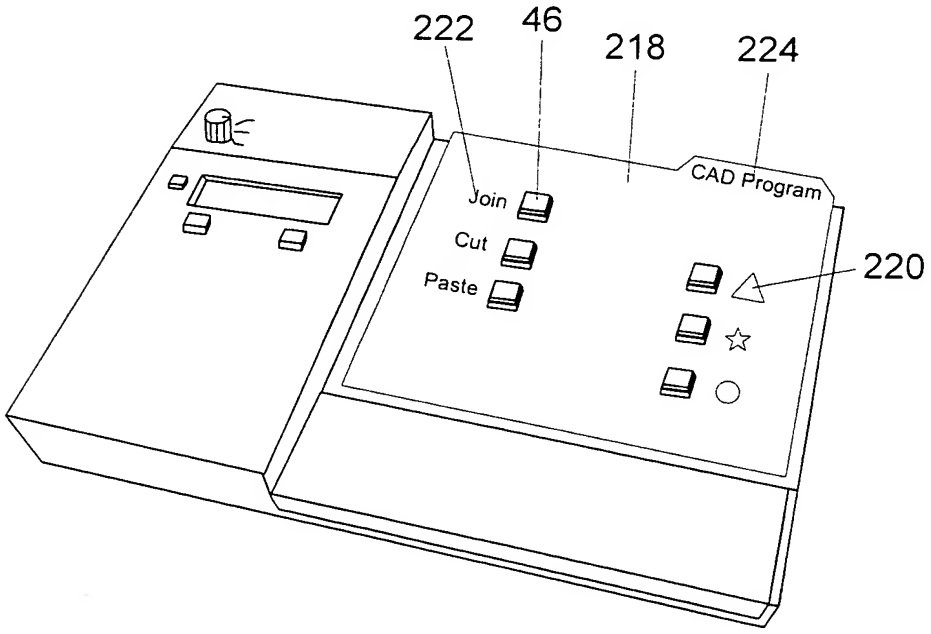
222
46
218
224
CAD Program
Join
Cut
Paste
220

Fig. 26

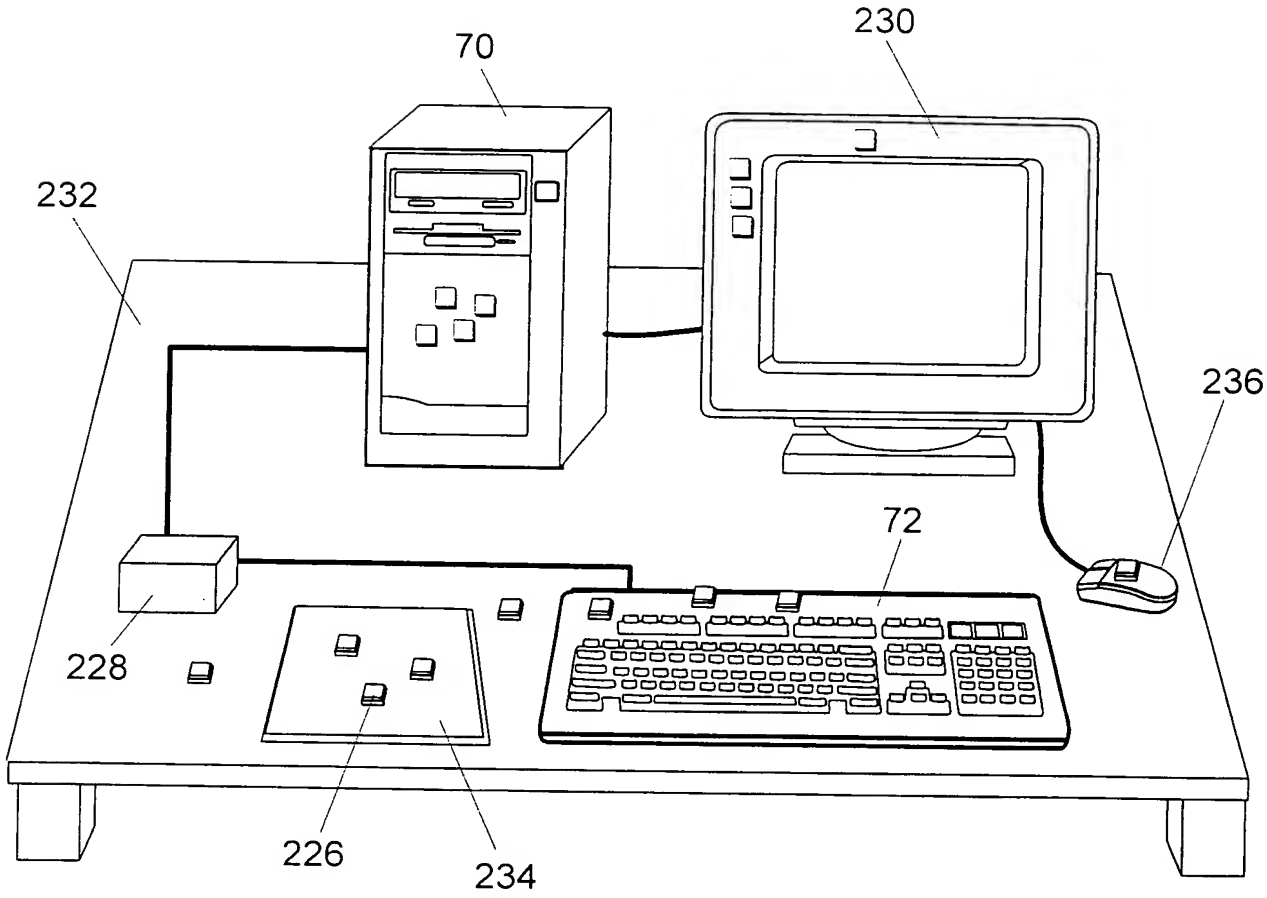

Fig. 27